12. Waveshaping Circuits and Data Converters
12.1 Comparators and Schmitt Trigger Circuits

Comparators

Comparator – a circuit, which compares two signals and produces a logic output signal, whose value (high or low) depends on which of the two signals is the largest.

The comparator is in fact a differential amplifier with high gain and limited maximum and minimum levels of the output signals.

![Circuit symbol for the comparator. If \( v_1 > v_2 \), then \( v_o \) is high; if \( v_1 < v_2 \), then \( v_o \) is low.](image)

![Transfer characteristics of ideal comparators.](image)

![Transfer characteristic of a real comparator.](image)

Except non-ideal transfer characteristic the comparator suffers from offset voltage, bias current and offset current.
Schmitt Triggers

Figure 12.5 The input voltage $v_{in}$ is compared to the reference voltage $V_r$.

Figure 12.6 Noise added to the input signal can cause undesired transitions in the output signal.
Assume that output voltages of the comparator are +10V and −10V.

If $v_{in} < -1V$, $v_o = +10V$ and the voltage at +input of the comparator is +1V. If $v_{in}$ increases, $v_o$ stays 10V as long as $v_{in} < +1V$.

If $v_{in} > +1V$, $v_o = -10V$ and the voltage at +input of the comparator is -1V. If $v_{in}$ decreases, $v_o$ stays -10V as long as $v_{in} > -1V$.

Thus for $-1V < v_{in} < +1V$ the output voltage could be +10V or −10V depending on the history of the process. The circuit exhibits hysteresis.

Figure 12.7 A Schmitt trigger is formed by using positive feedback with a comparator.
Variations of the Schmitt Trigger Circuits

Figure 12.8 Non-inverting Schmitt trigger.

Figure 12.9 Schmitt triggers that can be designed to have specified thresholds.
12.2 Astable Miltivibrators

**Multivibrator** – switching oscillator, producing non-sinusoidal signal (usually it produces rectangular pulses).

**Example 12.2 Astable - Multivibrator Analysis**

Find one expression for the frequency of the switching oscillator of Figure 12.16a. Neglect the input current of the comparator.

**Solution:**

\[
 v_c(t) = K_1 + K_2 e^{-t/RC} \tag{12.4}
\]

\[
 v_c(0) = -A/2
\]

\[
 v_c(0) = K_1 + K_2
\]

\[
 K_1 + K_2 = -A/2 \tag{12.5}
\]

\[
 v_c(\infty) = +A \quad \text{and} \quad v_c(\infty) = K_1 \Rightarrow K_1 = A
\]

\[
 K_2 = -3A/2
\]

\[
 v_c(t) = A - \left(3A/2\right)e^{-t/RC} \tag{12.6}
\]
\[ v_c(t) = A - \left(\frac{3A}{2}\right)e^{-t/RC} \quad (12.6) \]

\[ v_c(T/2) = \frac{A}{2} = A - \left(\frac{3A}{2}\right)e^{-T/2RC} \]

\[ e^{-T/2RC} = \frac{1}{3} \]

\[ -\frac{T}{2RC} = -\ln 3 \]

\[ T = 2RC \ln(3) \]

\[ f = \frac{1}{2RC \ln(3)} \quad (12.7) \]

**Figure 12.17** Waveforms of Figure 12.16b with \( t = 0 \) at the start of a positive half-cycle of \( v_o(t) \).
12.6 Sample - and - Hold Circuits

Sample-and-hold circuit (track/store; track-and-hold): a circuit which remembers the instantaneous value of the signal and stores it for a prescribed time to be measured (converted into digital form).

Tracking state: the output signal follows the input signal.

Hold state: the output signal is constant and stores the value of the input signal at the end of the sampling time (at the end of the tracking state).

Acquisition time: time at the beginning of the sampling state for which the output equalizes with the input.
12.8 Data Conversion

Analog-to-Digital Conversion

Analog-to-digital conversion: conversion of the signal from analog to digital form. From continuous function in time domain it is converted to a sequence of numbers, representing the signal levels at equidistant moments.

1. Sampling the signal by using sample-and-hold circuit.

2. The whole magnitude range of the signal is divided in $2^n$ zones ($n$ is the number of the bits). For each sample is determined the zone, in which it falls, and a corresponding code is generated.

Sampling theorem: to be possible to restore the signal from the sequence of the numbers, the sampling frequency must be at least twice more than the maximal frequency in the spectrum of the signal.

Sampling frequency $f_s = 1/T_s$; $T_s$ – the time between two consecutive samples.

![Analog-to-Digital Conversion](image)
Digital-to-Analog Conversion

Figure 12.40 The DAC output is a staircase approximation to the original signal. Filtering removes the sharp corners. *(Note: In addition to smoothing, the filter delays the signal. The delay is not shown.)*
12.9 Digital-to-Analog Converters (DAC)

Weighted - Resistance DACs

\[ i_i = \frac{V_{\text{ref}}}{R} 2^{-i+1} \]

\[ v_o = -R_f i_o = -D V_{\text{ref}} \]

Figure 12.41 Circuit symbol for a digital-to-analog converter.

Figure 12.42 DACs can be implemented using a weighted-resistance network. (Note: If \( d_i = 1 \), the corresponding switch is to the right-hand side. For \( d_i = 0 \), the \( i \)-th switch is to the left-hand side.)
12.9 Analog-to-Digital Converters

The Dual - Slope ADC

When $S_1$ is connected to $-v_s$: $v_x(t) = \frac{1}{RC} \int_0^t v_s \, dt = \frac{v_s}{RC} t$

The peak voltage at the end of $T_1$: $V_{peak} = \frac{v_s T_1}{RC}$

During $T_2$ the slope is constant and

$T_2 = \frac{V_{peak}}{|slope|} = \frac{v_s T_1 / RC}{V_{ref} / RC} = \frac{v_s T_1}{V_{ref}}$

$T_2$ is proportional to $v_s$. By measuring of $T_2$ the counter in fact measures $v_s$. 

Figure 12.50 Dual-slope ADC.