A 3.6 GHz Double Cross-Coupled Multivibrator VCO With 1.6-GHz Tuning

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Abstract—This brief presents a fully monolithic voltage-controlled oscillator (VCO) based on double cross-coupled multivibrator architecture with a speed enhancing RL-load designed and implemented on a standard 0.35-μm BiCMOS process. The tuning range achieved is greater than 1.6 GHz with a center frequency of 3.6 GHz and the measured phase noise is −98.2 dBc/Hz at an offset frequency of 600 kHz. The VCO draws 17.5 mA from a 2.4 V supply.

Index Terms—BiCMOS technology, multi-GHz VCO, wide tuning range.

I. INTRODUCTION

Relaxation oscillator-based voltage-controlled oscillators (VCOs) are widely used in applications where a large tuning range is needed. However, the phase noise performance of the relaxation oscillator is generally much lower than the phase noise performance of resonator tank based LC VCOs, even when the LC-tank is realized using low quality factor inductors and varactors. The main advantage of relaxation oscillators compared to LC VCOs is their broader tuning range.

From the literature on relaxation-type oscillators [1]–[3] it can be seen that active switching device parasitics are the limiting factor of maximum frequency for this type of oscillator. In this brief, in addition to the active pull-down technique [4]–[6], which was introduced in the context of multivibrators in [7], [8], another well-known method, peak shunting [9], is shown to be useful in reducing switching time and so increasing the maximum possible oscillation frequency of the circuit, while still giving reasonable output power.

In Section II, the effects of using traditional shunt peaking enhancement for switching delay reduction and loop bandwidth extension are analyzed briefly. In Section III, the simulation and measurement results of a double cross-coupled multivibrator VCO, designed using CADENCE tools and implemented on ST Microelectronic’s 0.35-μm BiCMOS technology, are presented and in Section IV, the measured results are compared to those of other published relaxation-type oscillators.

II. USING THE RL-LOAD IN DOUBLE CROSS-COUPLED MULTIVIBRATOR

A. Frequency-Domain Analysis

Bandwidth extension of an amplifier by adding a zero [9] is known also as shunt peaking. Here it is used to extend the bandwidth of our multivibrator circuit. Fig. 1 shows the schematic of a double cross-coupled ICO with RL-load and equivalent collector node capacitance.
**Fig. 3.** Double cross-coupled multivibrator VCO.

**Fig. 4.** Measured phase noise: $V_{CC} = 2.4$ V, $I_{CC} = 17.5$ mA, and $V_{Cent} = 1.2$ V.

**Fig. 5.** Simulated and measured tuning curves.

**Fig. 6.** The chip micrograph of the implemented circuit.

### TABLE I

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Simulated</th>
<th>Measured</th>
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<tbody>
<tr>
<td>$V_{CC}$ [V]</td>
<td>2.4</td>
<td>2.4</td>
</tr>
<tr>
<td>$I_{CC}$ [mA]</td>
<td>17</td>
<td>17.5</td>
</tr>
<tr>
<td>$f_c$ [GHz]</td>
<td>3.92</td>
<td>3.61</td>
</tr>
<tr>
<td>$\Delta f$ [GHz]</td>
<td>1.6</td>
<td>1.62</td>
</tr>
<tr>
<td>$P_{out}$ [dBm]</td>
<td>-7</td>
<td>-14</td>
</tr>
<tr>
<td>Phase noise [dBc/Hz]</td>
<td>-97 @ 600 kHz</td>
<td>-98.2 @ 600 kHz</td>
</tr>
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</table>

seen at the collector node and $L$ is the inductor value. When only a resistor is used, calculation of the impedance of the collector load circuit gives

$$|Z_{RC}(j\omega)| = \sqrt{\frac{R_C^2}{1 + \omega^2 R_C^2 C_{eq}^2}} \quad (1)$$

and

$$|Z_{RL c}(j\omega)| = \frac{R_C^2 + \omega^2 L^2}{\left(1 - \omega^2 L C_{eq}^2 \right)^2 + \left(\omega R_C C_{eq} \right)^2} \quad (2)$$

when an inductor is also used.

Using $R_C = 40$ $\Omega$, $L_C = 1$ nH, and $C_{eq} = 1$ pF the plots of (1) and (2) seen in Fig. 2(a) can be obtained. We can clearly see the bandwidth extension caused by adding an inductor into the circuit thereby adding one zero into the equivalent collector impedance function.

**B. Pulse Shaping Effects of $RL$-Load**

The switching transients can be estimated by calculating the current step responses of the collector load. For the $RC$-load, we can, after some calculation, write the differential pulse in the collectors as

$$v_d(t) = I_{TOT} \cdot R - 2 I_{TOT} \cdot R \cdot e^{-\frac{t}{\tau_{eq}}} \quad (3)$$

In the case of the $RL$-load for the rising voltage pulse front we get

$$v_1(t) = V_{CC} - R \cdot i_1(t) - L \frac{di_1(t)}{dt} \quad (4)$$
Assuming the final current through the inductor is $I_{\text{TOT}}$ and initially $i_1(t) \equiv 0$ yields

$$i_1(t) = \left( I_{\text{TOT}} \cos(\omega_d t) + \alpha I_{\text{TOT}} \frac{1}{\omega_d} \sin(\omega_d t) \right) e^{-\alpha t} \quad (5)$$

and $\frac{di_1(t)}{dt}$ is

$$\frac{di_1(t)}{dt} = \left( \omega_d I_{\text{TOT}} - \frac{\alpha^2 I_{\text{TOT}}}{\omega_d} \right) \sin(\omega_d t) e^{-\alpha t} \quad (6)$$

In (5) and (6), $\omega_d$ is the damped resonance and $\alpha$ is the noper frequency of the equivalent collector load circuit given by

$$\alpha = \frac{R}{2L}, \quad \omega_d = \sqrt{\frac{\omega_0^2}{\alpha^2} - \omega_0^2}. \quad (7)$$

The equation for the falling voltage pulse front $v_2(t)$ has the same form except that the direction of current change is different giving

$$i_1(t) = I_{\text{TOT}} + \left( -I_{\text{TOT}} \cos(\omega_d t) - \frac{\alpha I_{\text{TOT}}}{\omega_d} \sin(\omega_d t) \right) e^{-\alpha t} \quad (8)$$

and

$$\frac{dv_2(t)}{dt} = \left( \omega_d I_{\text{TOT}} - \frac{\alpha^2 I_{\text{TOT}}}{\omega_d} \right) \sin(\omega_d t) e^{-\alpha t}. \quad (9)$$

The differential voltage pulse front can be now approximated as

$$v_d(t) = v_1(t) - v_2(t). \quad (10)$$

In Fig. 2(b) the differential pulse fronts given by 3 and 10 are plotted using the values mentioned earlier and we can clearly see that the use of the $RL$ load both speeds up the switching and enhances the amplitude. The $Q$ factor of the inductor is not critical since the series resistance $R$ dampens the response in any case.

### III. Design and Implementation of the Double Cross-Coupled VCO With ST-$\mu$E 0.35-$\mu$m BiCMOS Technology

The schematic of the double cross-coupled multivibrator VCO designed in this work is shown in Fig. 3. The inductors on the collectors of the transistors $Q_1$ and $Q_2$ are realized as a center tapped coil. The inductance of both inductors is about 0.65 nH and the coupling between them is about 0.32. These values were obtained using ASITIC software [13].

The resonance tanks on top of the current mirror transistors $Q_9$ and $Q_{10}$ are inserted to enhance the output impedance of these devices. The inductors are 1.4-nH inductors provided by the foundry.

A simple PMOS differential pair is used to create the differential control currents. These are equipped with a degeneration resistor to improve the linearity and, in order to achieve single-ended control the second input is biased with a simple resistive voltage divider. The current through the differential amplifier and also the current through the core circuit can be controlled by the $V_{\text{bias}}$ voltage. The output signal is taken from the active pull-down emitter followers.

After parasitic extraction the simulated center frequency was 3.92 GHz with 1.6-GHz tuning. The simulated phase noise with the control voltage of 1.0 V was $-97$ dBc/Hz at 600-kHz offset frequency. The simulated single-ended output power was $-7$ dBm. The total current consumption was 17 mA from the 2.4-V supply.

The circuit was measured directly on the wafer using a HP4352A VCO/PLL signal analyzer with a HP70427A microwave downconverter and a Rohde & Schwarz FSEM30 spectrum analyzer. The measured center frequency was 3.61 GHz at a tuning range of 1.62 GHz. The measured single-ended output power was $-4$ dBm and the measured phase noise was $-98.2$ dBc/Hz at 600-kHz offset frequency with a control voltage of 1.0 V. The measured phase noise at $f_{\text{max}}$ and simulated and the measured tuning curves are presented in Figs. 4 and 5, respectively. The simulated and measured results are summarized in Table I. The chip micrograph is shown in Fig. 6.

### IV. Comparison

Table II presents references to some published papers on relaxation oscillators [11–13], [11] from the beginning of the 1990s up to the present. These indicate that the double cross-coupled VCO with the $RL$ load is capable of working at high frequencies. Compared to the traditional negative $g_m$ oscillators the architecture has a higher phase noise but in the category of relaxation oscillators it displays fairly good performance.

### V. Conclusion

The advantages of the double cross-coupled multivibrator have been considered briefly as well as use of $RL$ loading to increase the switching speed. The simple analysis showed that the series inductor improves the switching time. The simulation and measurement results of the double cross-coupled VCO implemented on the ST-$\mu$E 0.35-$\mu$m BiCMOS processes have been presented and are seen to be well correlated. Measurements showed that the tuning range can be broadened substantially but the control stability will need to be given more consideration in the future in order to lower the phase noise. Some comparison with other relaxation-types of VCOs was made showing that the double cross-coupled VCO can operate at gigahertz frequencies giving a wide tuning range and fairly low phase noise.

### REFERENCES


Min/Max Circuit for Analog Convolutional Decoders

Brent Maundy

Abstract—A novel minimum or maximum compare and select circuit is presented in this brief for use in analog convolutional decoders. Based on voltage difference circuits coupled to a decision circuit the proposed circuit can differentiate voltages of 10-mV differences in the simple configuration or 5 mV in an improved configuration. Simulation results indicate an operational speed of 100 MHz/s of a 3.3-V supply, which is comparable to or 5 mV in an improved configuration. Simulation results indicate an operational speed of 100 Mbits/s of a 3.3-V supply, which is comparable to higher speeds and consume less power than their digital counterparts. Recently they have been used in read channels of state-of-the-art magnetic recording systems [16]–[18]. A necessary and powerful component of many of these decoders (Digital or Analog) is the add–compare–select (ACS) block [8], [9], [19], which has been shown to create the speed bottleneck in these decoders [19]. Its main function is to add a data dependent branch metric (error) $B_{i,j,n}$ (i and j are states) to a path metric $M_{i,n}$ and compare the result over a set of states $i$ at sample time $n$. That is

$$M_{i,n} = \min_{i} [M_{j,n-1} + B_{i,j,n}]. \quad (1)$$

If a 2-state trellis or dicode system is used and $\{i\} = \{0, 1\}$, the compare and select portion of the ACS block needs to determine the minimum of two summed quantities. In [5], [8], and [9] innovative comparators were proposed that perform the ACS task in a fast and efficient manner. Current differences as small as 1-$\mu$A were reported which appear to far exceed previously reported analog Viterbi decoders. In this brief we report up on a min/max circuit that may be used as a possible CS component. Inspired by the work of [5], [6], [8], [9] the circuit functions by actually computing the difference between two voltages and using that difference to determine the minimum or maximum of the two quantities. Two difference circuits are employed to determine the difference and a decision circuit compares the magnitude of the difference with zero. However, unlike its voltage [2], [3], [15] or current counterparts [5], [8], [9] our proposed circuit uses only two devices between the rails to achieve comparable speeds (> 100 Mbits) with its current counterparts. Throughout the paper we assume that the variables to be compared are functions of time but the time notion has been omitted for simplicity to illustrate the CS operation.

II. CIRCUIT DESCRIPTION

The proposed circuit is shown in Fig. 1. It consists of level shifters formed by NMOS transistors M1–M6, M7–M12 and a decision circuit formed by the PMOS transistors M13–M16. The action of the level shifters is to form two difference circuits whose inputs are the same but reversed in polarity connections. A lone NMOS transistor MR acts as a reset switch to force the node voltages at $V_{x}$ and $V_{y}$ to be the same after the minimum input voltage is determined. The same nodes are connected to CMOS inverters that selectively switch via transmission gates, the voltage inputs depending on the voltages at nodes $V_{x}$ and $V_{y}$. For the moment let us assume that all the transistors except MR have their bulks tied to their sources so that bulk effects can be ignored. MR’s bulk is tied to ground potential. In addition, the NMOS transistors are sized equally so that any given series connected pair will have the same drain current and, therefore, the same gate to source voltage. A bias voltage $V_{bias}$ is applied to transistors M1, M5, M7, and M11 and it is assumed that $V_{bias} > V_{Tn}$, where $V_{Tn}$ is the threshold voltage of all the $n$-transistors. If transistors M2 and M8 are supplied with gate voltages $V_{1}$ and $V_{2}$ such that $V_{1} > 2V_{Tn}$, it follows that the voltages at the sources of M2 and M8 will be $V_{1} = V_{bias}$ and $V_{2} = V_{bias}$, respectively. By a similar reasoning the source voltage of M10 and M4 will be at potential $V_{1} = V_{bias}$ unless $V_{1} > V_{2}$ or $V_{2} = V_{bias}$ if $V_{2} > V_{1}$, respectively. At this point depending on the relative magnitude of

References


Minimum and maximum circuits have shown themselves to be useful building blocks in many applications such as neural networks, digital signal processing, and fuzzy logic [1], [2]. When employed in artificial neural networks they traditionally take the form of winner-take-all (WTA) [3]–[6] or loser-take-all (LTA) [7] circuits. A WTA circuit can be regarded as a competitive network that chooses the maximum value out of a number of inputs. LTA circuits are multiple input versions of minimum function circuits. An emerging application of minimum function circuits is in the area of analog Viterbi decoders to decode convolutional codes [8]–[14]. Traditionally the Viterbi algorithm (VA) has been implemented with digital circuits because of the ease of computation and implementation. However as the size of the trellis grows this can place some stringent memory and speed requirements on the digital circuits used. Analog implementations of the VA on the other hand have been shown to only require about 6 bits of accuracy and can be made relatively fast [15]. They also have the potential to operate at higher speeds and consume less power than their digital counterparts.