High-Performance Differential VCO Based on Armstrong Oscillator Topology
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Abstract—A symmetric topology based on the classical Armstrong's oscillator was developed and implemented as a fully monolithic voltage-controlled oscillator using ST Microelectronics' 0.35-μm BiCMOS process ($f_T = 35$ GHz). It oscillates at a center frequency of 4.4 GHz, has a tuning range of 1.0 GHz, delivers a single-ended output power of $-6.5$ dBm, and the minimum current consumption is less than 4 mA from a 2.5-V power supply. The phase noise is $-125$ dBc/Hz, measured at 3-MHz offset.

Index Terms—BiCMOS technology, multi-GHz VCO, wide tuning range.

I. INTRODUCTION
The huge growth in the production volumes of high-performance and low-cost wireless and optical communication units (mobile phones, W-LAN, O-LAN, etc.) has led to strong demand for fully monolithic solutions in low-cost integrated technologies [1]–[5]. The major difficulties with full integration concern mainly the voltage-controlled oscillator (VCO) and power amplifier (PA). It seems that the VCO is much nearer to full integration using the present achievements in silicon technologies.

II. CIRCUIT TOPOLOGY
In this work, the classical Armstrong oscillator [6], [13] is modified in order to achieve fully monolithic and differential realization, here referred to as the symmetrical Armstrong voltage-controlled oscillator (SA-VCO), which is presented in Fig. 1. A similar basic idea but with a different topology was used in [7]. In our work, taking the oscillation signal from the core of the VCO in a different manner further enhances the pulling figure. We also connect an inductor between the emitter branches of the differential pair and the output node of the simple current mirror formed by Q3 and Q4 to improve the differential-pair common-mode rejection ratio (CMRR). The idea of the emitter inductor was introduced in an earlier work of ours [8]. The benefits of integrated inductors and transformers over resistors certainly are:

1) high gain in the vicinity of the resonance frequency while frequencies not of interest (noise) are much less amplified;

2) lowered power supply still produces higher swing of the voltage output;

3) an emitter coil enhances the output impedance of the current mirror and thus the CMRR of the differential stage;

4) in symmetric stages due to the mutual inductance, the decrease in current in one branch of the transformer will stimulate an increase in current in the other branch making the stage faster;

5) mutual inductance leads to a smaller physical size for the transformer with the same inductance thus contributing to an improvement in the $Q$-factor;

6) a differentially driven inductor has both the $Q$-factor and the self-resonance frequency nearly doubled compared to a single-ended driven inductor [9].

III. OPERATION AND DESIGN OF THE SA-VCO
The operational principle of the circuit is based on the classic Barkhausen criterion where the cross-connected differential pair provides the negative resistance. The bias of transistors Q1 and Q2 is fed from the center-tap of a secondary coil of the transformer. The power supply is coupled to the center-tap of a primary coil of the transformer, which together with the pn-junction varactors form the collector loads of Q1 and Q2. For low phase noise, a high $Q$-factor of the resonator and high oscillation amplitude is required [10]. The amplitude can be further increased by increasing the bias current, but at the expense of greater power consumption. The voltage $V_{dc}$ at the center tap of the TF can be adjusted to avoid the increase in phase noise caused by the forward bias of the base–collector junction. The main losses and reduction in $Q$-factor are primarily due to
parasitic capacitance between the inductor and substrate, metal losses of the inductor windings at lower frequencies, skin effect at high frequencies, eddy currents, and substrate losses due to a relatively highly doped substrate [11]. To overcome these problems at high frequencies, smaller inductor areas were favored, the inner turns of the coils were omitted, and only the uppermost metal was used for inductors.

The scaling of transistors was done keeping in mind noise issues, parasitic capacitances, and current gain and density. Device noise sources include thermal, shot, and 1/f noise, which dominates at lower frequencies. The phase noise of the VCO is partly due to this 1/f noise, which is upconverted into the operating frequency band. The 1/f noise corner was simulated for several types of transistors, concurrently checking the fT and current gain curves of the transistors in order to find the optimum size and shape. Low thermal noise due to the base resistance requires a larger transistor at the expense of higher current consumption. Large transistors may also suffer from the degradation in noise performance at gigahertz frequencies because the transistor current gain begins to decrease.

The output is taken from the emitter resistors and fed to a buffer stage. The use of emitter degeneration resistors enhances the pulling figure by about a factor of two. However, the phase noise increases due to additional noise generated by the resistors. The simulations showed that the phase noise was increased by +4 dB at 3-MHz offset. This could be avoided by using inductors instead of resistors. The output impedance of the CM can be modeled as a large resistor in parallel with a small capacitor, which causes the common-mode gain to rise by +6 dB/octave at high frequencies [12]. The emitter inductor cancels out the transfer-function zero caused by the parasitic capacitors at the collector node of the CM output transistor and thus also cancels out the increase in the common-mode gain. The output transistor of the CM should be kept as small as possible in order to minimize those parasitic capacitors and to maintain the high output impedance.

IV. A SYNCHRONOUSLY TUNED BUFFER APPROACH

The buffer is needed to drive off-chip 50-Ω loads and could be omitted if the transceiver is fully integrated. In addition, it isolates the core of the SA-VCO from the load, thus enhancing a load-pulling figure. The realized buffer is a differential amplifier that works with a reduced bandwidth and is controlled together with the VCO. Since the transformer is not ideal, it has a relatively poor coupling. Thus, the output power suffers but the load has less influence on the oscillation frequency, i.e., the pulling figure of the VCO is improved.

V. SIMULATION RESULTS

After the initial values were designed, the SA-VCO circuit was simulated with CADENCE Spectre RF. The inductors and transformers were designed using the tool ASITIC. The nominal power consumption of the SA-VCO from a 2.5-V power supply is less than 10 mW (without the buffer and control blocks) when the circuit produces a differential output signal of 600 mVp-p at 4.9 GHz. The tuning range is 1.0 GHz with a supply of 2.5 V. The pulling figure is 5.4 MHz, which is more than two times better than the pulling figure of 12 MHz obtained when the output of the VCO is taken from the bases of Q1 and Q2 without emitter degeneration resistors (voltage standing wave ratio, VSWR = 2). The single-ended output power to a 50-Ω load equals −6.5 dBm and is relatively constant over the whole frequency range. The simulations were done with a total supply current of 18 mA. If the SA-VCO is used in a fully integrated transceiver, it consumes only 4 mA (i.e., the core of the VCO consumes only 4 mA).

VI. MEASUREMENTS

Measurements of the SA-VCO (Fig. 2) were made on a Cascade Summit-9000 probe station. The tuning curve and output power were measured using a Rohde & Schwartz FSEM30 spectrum analyzer. Other measurements were carried out using a HP4352B VCO/PLL signal analyzer with a HP70427 microwave downconverter. The measured results indicated with a solid line and the simulated curves with a dash-dot line are very close to each other. The measured tuning range is 1000 MHz with a total slope of 355 MHz/V (Fig. 3). The single-ended output power to the 50-Ω load
equals $-8 \text{ dBm}$ and is presented together with the simulated values in Fig. 4. When the insertion losses of the output cable (1.16 dB between 3.6 and 5.4 GHz) and the HP11742 blocking capacitor (0.3 dB) are taken into account, the real output power equals $-6.5 \text{ dBm}$ as was simulated. The SA-VCO has a phase noise of $-102.5 \text{ dBc/Hz}$ at 600-kHz offset and $-125 \text{ dBc/Hz}$ at 3-MHz offset at a frequency of 4.7 GHz (Fig. 5). There is a substantial difference between phase-noise simulations and measurements since the simulations were carried out using the standard bipolar model instead of the high-precision models.

VII. ANALYSIS OF THE RESULTS AND CONCLUSION

The simulated and measured frequency ranges match very closely. The phase noise of the SA-VCO can be improved, and still maintain the enhancement of the pulling figure by using emitter inductors instead of resistors.

REFERENCES