Algorithms and Implementation Platforms for Wireless Communications
TLT-9706/ TKT-9636 (Seminar Course)

BASICS OF FIELD PROGRAMMABLE GATE ARRAYS

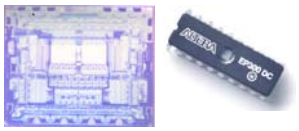
Waqar Hussain
firstname.lastname@tut.fi
Department of Computer Systems
Tampere University of Technology

Lecture Contents

1. Why there was a need for FPGA ?
2. What is the Scope of FPGA usability ?
3. How to Implement a Digital System ?
4. FPGA Architecture
5. The Unit of Structure of FPGA
6. Hardware Description Languages
7. Synthesis / Place and Route
8. Timing, Area and Power Analysis
9. Future of FPGA Technology

Why there was a need for FPGA ?

- Before Programmable Logic?
  - Fixed hardware = Fixed usability
  - Limited flexibility only possible by adding software support, for example *processors*
  - Upgrade or alteration in hardware logic was not guaranteed
  - An upgrade meant a completely new system
- World's First Programmable Logic Device (PLD)
  - EP300: 320 Gates, 3-µm CMOS
  - 10-MHz Performance, 20 I/O Pins
  - Desktop Programming



3

Why there was a need for FPGA ?

The FPGA industry sprouted from programmable read-only memory (PROM) and programmable logic devices (PLDs). PROMs and PLDs both had the option of being programmed in batches in a factory or in the field (field programmable)

- World's First FPGA with Embedded RAM in 1995
- 100K Gates, 0.4 & 0.3 µm
- >10M Transistors
- 50-100 MHz Performance
- First PCI Integration
- First IP Partner Program

Xilinx Co-Founders, Ross Freeman and Bernard Vonderschmitt, invented the first commercially available field programmable gate array in 1985 – the XC2064

4

Why there was a need for FPGA ?

- With FPGAs
  - Reprogrammable Logic ⟶ reusability
  - Lower Non-Recurring Engineering (NRE) Cost
  - Good for Prototyping
  - Less Time to Market
  - Can act as a testing device for other digital circuits
  - Economical to be used for small volumes of products
  - Students can understand digital design concepts in a better way by designing their custom logic

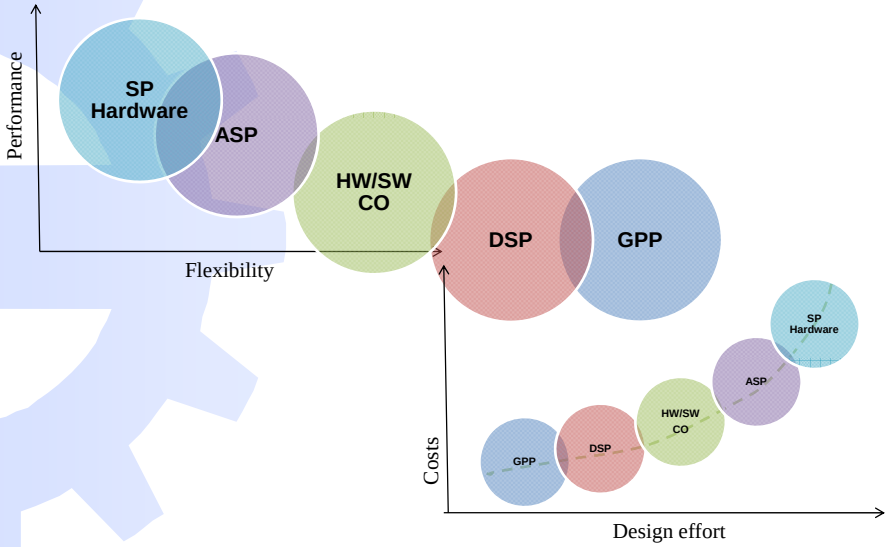
5

What is the Scope of FPGA usability ?

- Home Appliances
- Communication Systems
- Control Systems and Automation
- Mechanical and Civil Engineering
- Test and Measurement Industry
- Medical Equipment
- Avionics and Aerospace Application
- Academia

6

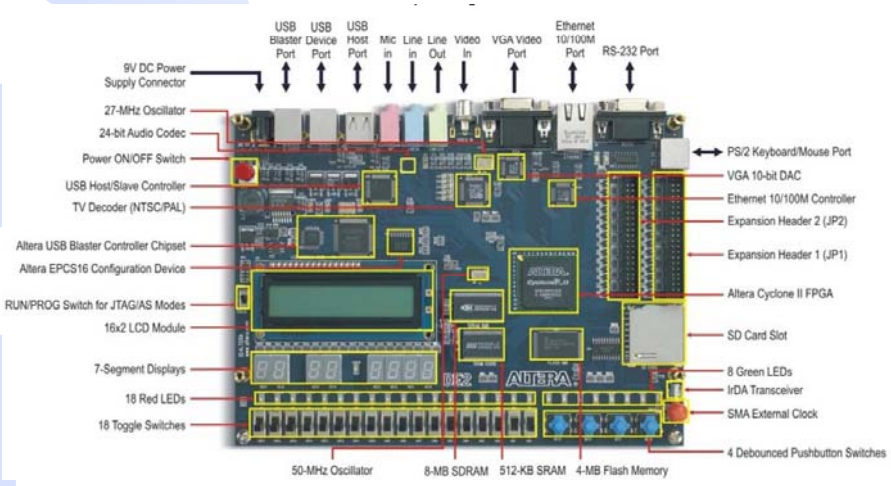
How to Implement a Digital System ?



7

FPGA Architecture

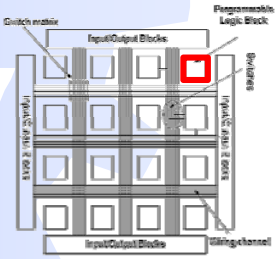
- An Example of FPGA Prototyping Board

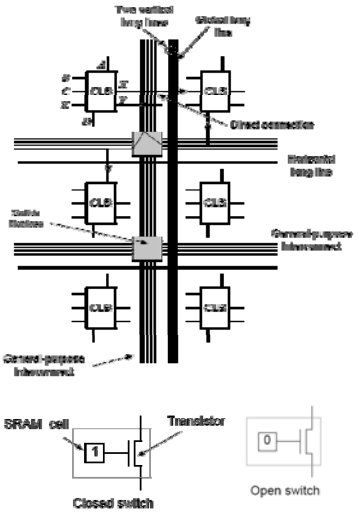


8

FPGA Internal Architecture

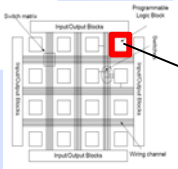
- The CLB exchange data using local and global interconnects
- Local Interconnects >> Global Interconnects
- Other than CLBs the interconnects are also programmable

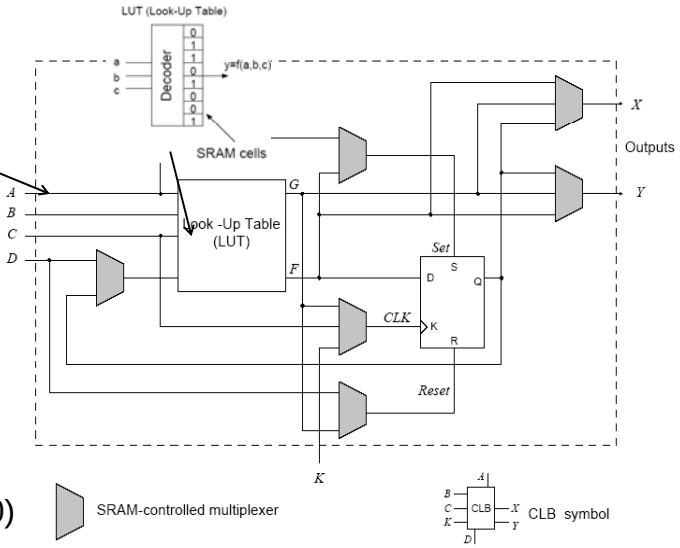




9

Basic Unit of FPGA Configurable Logic





The unit is
"CLB" –Xilinx
"LE" - Altera

(Example: Xilinx XC2000)

10

Hardware Description Language

- Can we use C as HDL?
  - Operations performed in a sequential order
  - Help human's thinking process to develop an algorithm step by step
  - Resemble the operation of a basic computer model
- Characteristics of digital hardware
  - Connections of parts
  - Concurrent operations
  - Concept of propagation delay and timing
  - Characteristics cannot be captured by traditional PLs
  - Require new languages: HDL

Modern HDL

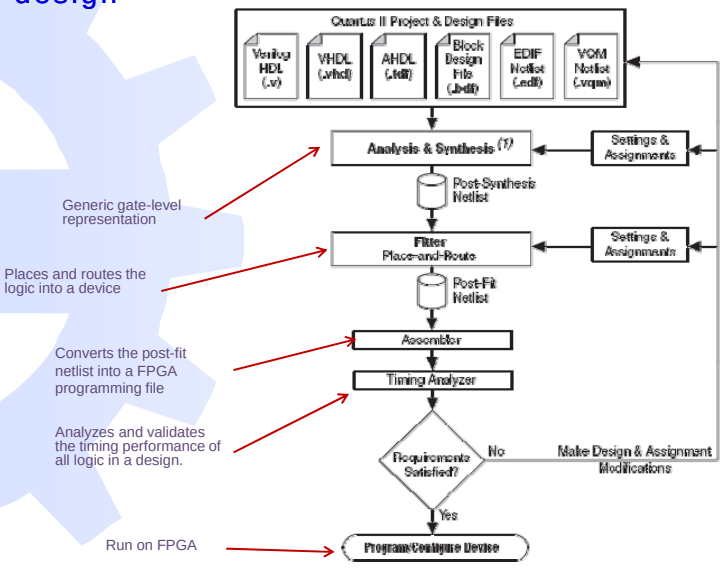
- **Capture Characteristics of a Digital Circuit**
  - Entity & Connectivity
  - Concurrency & Timing
- **Cover Description**
  - In Gate Level and RT Level
  - In structural view and behavioral view
    - Behavioral View
      - Describe functionalities and I/O behavior
      - Treat the system as a black box
      - Corresponds to a sequential PL
    - Structural View
      - Describe the internal implementation (components and interconnections)
      - Essentially block diagram

Synthesis, Place and Route

- **Accepts HDL description of a system (VHDL, Verilog)**
- **Quartus II (A Synthesis Tool) Flow Phases**
  1. Setup
  2. Perform RTL Synthesis
  3. Map basic gates into FPGA logic
  4. Place the logic into specific location in chip
  5. Route (connect) the logic elements together
  6. Provide statistics and analysis results
  7. Create a programming file and upload it into the FPGA

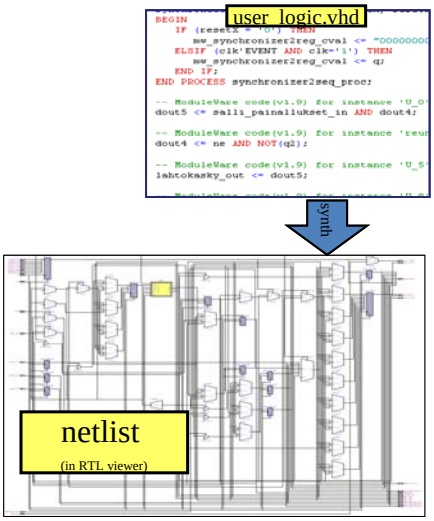
Synthesis, Place and Route

Quartus II design flow after simulated and verified design



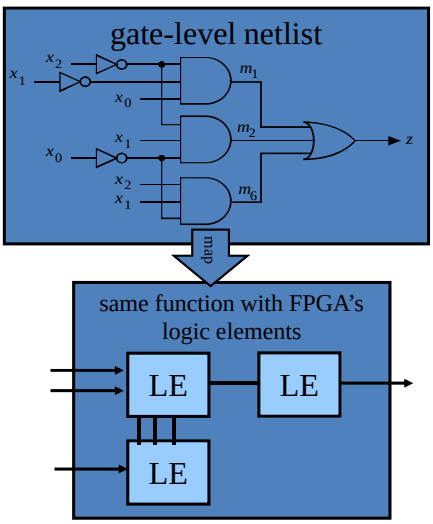
Synthesis, Place and Route
RTL Synthesis Step

- **Synthesis**
  - Creates basic gates and DFFs from HDL
    - Result is so called *netlist*
  - A full description of logical ports and their connections
- **Synthesis results can be viewed with RTL Viewer Tool**



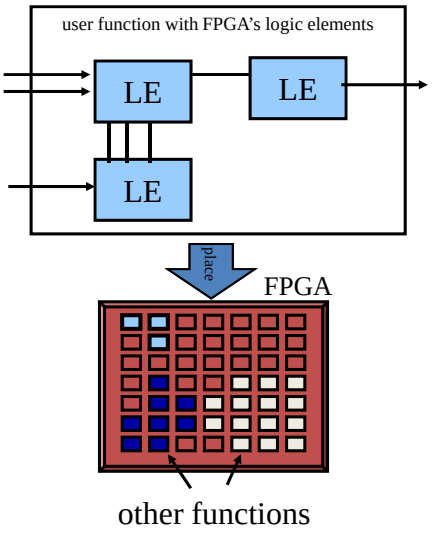
Synthesis, Place and Route
Technology Mapping

- Transforms the basic gates into technology specific components
- i.e. into logic elements (LE) with Altera FPGAs
- LE contains look-up table and DFF



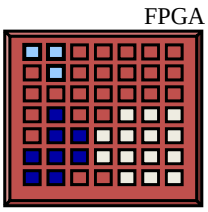
Synthesis, Place and Route
Placement

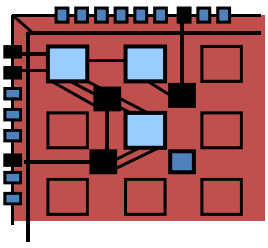
- Select which physical LE implement the user function
- Selected LE should be close
  - to each other
  - to physical IO pins that they use
- Other logic may complicate placement



Synthesis, Place and Route
Routing

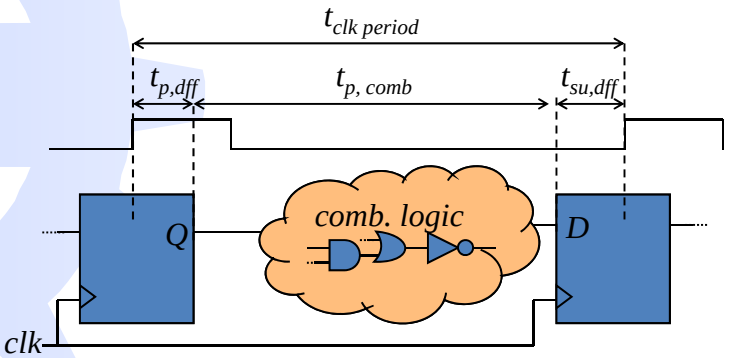
- Connects used LEs
  - together
  - to input/output pins
- FPGAs have programmable routing switches
- Sometimes detours are needed
- Algorithmically complex operation
  - May take a while with bigger systems





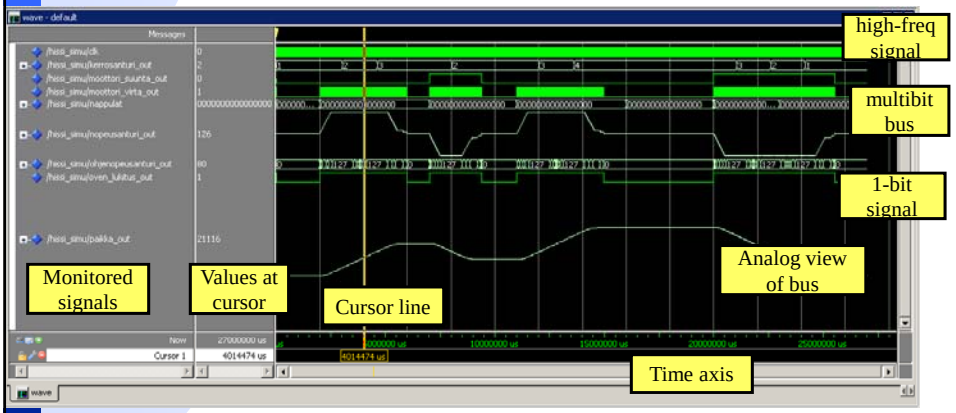
Timing, Area and Power Analysis

- After placement and routing, Critical Path is determined
- Critical Path is the one which is offering longest propagation delay on FPGA floor



Timing, Area and Power Analysis

ModelSim - Waveform



Timing, Area and Power Analysis

- It is important to analyze area utilization summary.
  - Design resources should not exceed FPGA resources
    - Design can be synthesized optimally w.r.t area utilization if does not fit by normal synthesis
- More exchange of data between memory and processing elements means more switching between the transistor states therefore more power dissipation
  - Two Important factors for obtaining power estimate
    - Accurate signal activity
    - Accurate power models
      - Provided by the FPGA Vendor

21

Future of FPGA Devices

- FPGA device densities are increasing in millions of gates
- Altera's latest device is Stratix-V
- Xilinx's latest device is Virtex-7
- Higher density devices are expected with higher number of hard macros
  - FPGA are expected to stay in market for the next 50 years
- Research interests are growing more towards Coarse-grain Reconfigurable Array (CGRA)
  - The unit of structure in FPGA is a LE whereas in CGRA, it is the ALU

22